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CTF3 Note 064 (Tech.)
(Timing)

ECL COUNTER CRATE FOR CTF3 PRECISION TIMING

J. P. H. Sladen

Abstract

An ECL counter system has been developed for precision timing applications in CTF3. One chassis can contain up to four drawers each containing four 24-bit counters. The system was designed to be clocked at 250 MHz but operation up to 400 MHz is possible. Each counter is followed by a fine delay circuit giving a 10 ps resolution. An interface is provided allowing full computer control.

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1 Introduction

The majority of timing pulses (modulators, klystrons etc.) required for CTF3 are obtained from Tg8 VME modules externally clocked at a sub-harmonic of the linac's 3 GHz RF [1]. These modules have an output jitter relative to the clock of about 170 ps rms. For some applications (e.g. thermionic gun timing) the Tg8's are followed by a VME delay module [2] developed for CTF3. This permits finer delay resolution (currently 200 ps) and, as it re-synchronizes the Tg8 output to the external clock, it is also able to produce a lower output jitter. This jitter has been measured at 72 ps rms. For applications requiring more precise timing, an ECL timing system has been developed and is described in this note. The applications include beam instrumentation (notably streak camera) and production of the phase coding timing both for the sub-harmonic bunchers and for the photo-injector.

The system consists of a stand-alone chassis that can contain up to four drawers each containing four 24-bit counters. They were designed to be clocked at 250 MHz but can run up to 400 MHz. Each is followed by a fine delay circuit with 10 ps resolution and 5 ns range. The output jitter of the counter with the fine delay set to zero has been measured at 1.1 ps rms. This value increases as the fine delay is added. The jitter is 1.6 ps rms for a fine delay setting of 2 ns. Auxiliary cards can be added to the chassis for level conversion, fan-out and pulse combination. A computer interface is provided for connection to a DSC.

2 General crate layout

The system is housed in a 6U Europa chassis. Front and rear views of the crate are shown in Figure 1. The front can house up to four counter drawers. The rear side houses the following:

- Two computer interface cards.
- 6 slots for either ECL/TTL converter or ECL combiner and fan-out cards as required.
- BNC patch-panel.
- Power supplies, 5V, -3.3V (x 2) and –5.2V.

The patch panel is used for connection of the external clock and trigger sources and for connection of the counter outputs. Internally, coaxial connections run from the counter drawer's backplane to the rear mounted patch panel. Each counter drawer has separate clock and trigger inputs. These are then common to all four counters within the drawer. All input and output signals are ECL levels. The clock inputs are AC coupled and can accept either 50 % duty cycle ECL levels or a sine wave, 3 dBm to 10 dBm.

The two computer interface cards allow connection of the crate to a parallel I/O card situated in a DSC for providing full computer control.

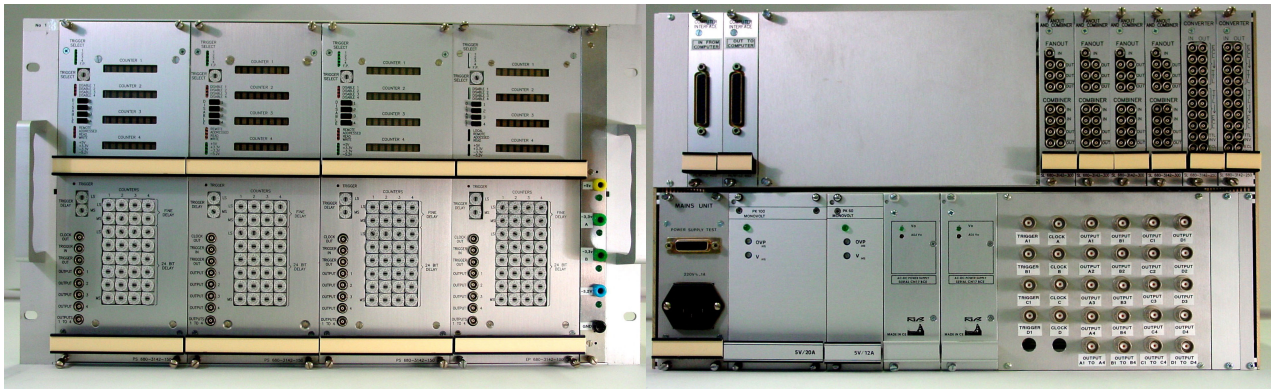

Figure 1: Front and rear views of crate.

3 24-bit counter drawer

The 6U 20TE drawer (Figure 2) contains a main board as well as a front panel mounted board for rotary switches and alphanumeric displays. The main board contains the four 24-bit ECL counters. Each consists of three cascaded 8-bit counter IC's. If 8 or 16 bits are sufficient, then one or two IC's can simply be left off the board, reducing power consumption. The counters are followed by 9-bit fine delay IC's that have a resolution of 10 ps. Control of trigger selection, disable and delay is achieved either locally via the front panel or remotely via the computer interface. The *ECLinPS Plus* series IC's are used for the counting and fine delay. PLD's are used for the control logic.

3.1 Front panel

The front panel contains the following:

a) 18 LED's for the indication of:

i) Currently selected trigger source (5).

ii) Trigger active (1).

iii) Counter disable status (on = disabled) (4).

iv) Power supply status (4, although +3.3V supply is unused).

v) Computer control status: LOCAL, ADDRESSED, WRITE and READ (4).

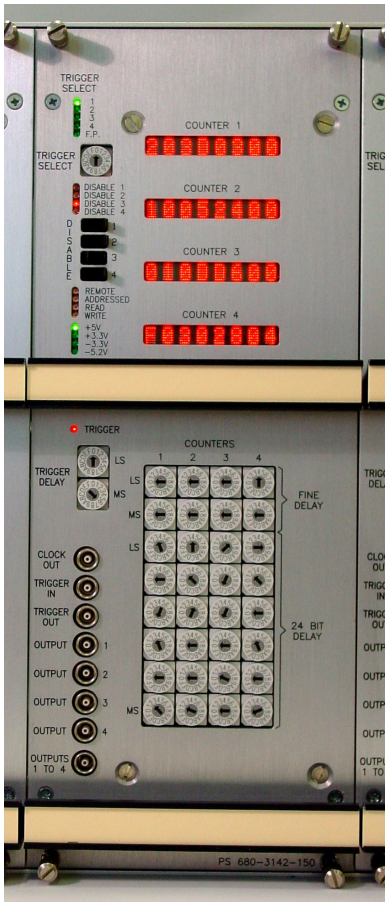

Figure 2: Front panel of counter drawer.

b) 4 single-pole switches for counter disable.

c) 35 HEX rotary switches for:

i) Trigger selection (1).

ii) Trigger delay (2).

iii) Counter delay (32). The two least significant switches of each counter control the fine delay with 20 ps resolution. There is no local control of the 10 ps step. The six most significant switches of each counter control the 24 counter bits.

d) 4 alphanumeric 8-character displays for HEX display of current delay setting of each counter. The six most significant characters of each display are the HEX representation of the 24 counter bits. The two least significant characters of each display are the HEX representation of the 20 ps bit to the 2560 ps bit of the fine delay setting (i. e. FF = 5100 ps). There is no local display of the 10 ps bit.

e) 8 Lemo connectors for the following ECL signals:

i) Clock monitor output (1).

ii) Front panel trigger input (1).

iii) Trigger monitor output (1).

iv) Counter outputs (one clock period long) (4).

v) Sum (OR) output of all four counters (1).

3.2 Rear connectors

The two rear 3 x 32 pin DIN backplane connectors contain the following:

a) Clock input (AC coupled ECL).

b) Four trigger inputs (ECL).

c) Computer control lines (8 address, 8 data and 3 control inputs, 8 data outputs).

d) Power supply inputs (+5 V, -3.3 V, –5.2 V and GND).

e) Outputs of each of the four counters (ECL, one clock period long).

f) Sum (OR) output of all four counters (ECL).

g) Fast disable input for each counter (ECL).

3.3 Trigger circuitry

All four counters share the same ECL start trigger. It can be selected from five sources: four on the rear connector and one on the front panel. Selection is done either locally via a front panel rotary switch or remotely via the computer interface.

During the first clock cycle after the rising edge of the trigger pulse, the delay settings are loaded into the counters and latched into the fine delay IC's. Counting commences in the next cycle.

For correct timing of the trigger with respect to the clock, each card contains a fine delay circuit in the trigger path. It is adjusted over a range of 5 ns in 20 ps steps by two front panel rotary switches. This adjustment needs only be performed at the setting-up of the crate and cannot be carried out remotely.

3.4 Counter disable

Each of the four counters can be individually disabled by front panel switches or computer control. In addition, a fast ECL disable (active high) is provided for each counter on the rear connector.

3.5 Dual-in-line switch setting

A 4-pole DIL switch is located on the main circuit board for setting of the board address and for override of the computer local/remote setting (Table 1). Pole 1 should normally be ON in which case selection of remote or local control is done by a control bit from the computer interface. When OFF, the card is under local control, irrespective of the state of the computer control bit. The PCB address bits should match bits A7, A6 and A5 of the computer control address byte (see Table 4).

POLE NUMBER	FUNCTION
1	LOCAL OVERRIDE (ON = NORMAL, OFF = OVERRIDE)
2	PCB ADDRESS 0 (ON = 0)
3	PCB ADDRESS 1 (ON = 0)
4	PCB ADDRESS 2 (ON = 0)

Table 1: PCB DIL switch functions.

4 Fan-out and combiner card

The card contains one ECL fan-out buffer and one combiner. The fan-out has four true and two complementary outputs. The combiner consists of an ECL OR gate followed by a buffer with two true and two complementary outputs.

5 Converter card

The card contains four TTL to ECL and four ECL to TTL converters. There is also one ECL and one TTL inverter. The TTL inputs are 50 Ω terminated and the outputs are 50 Ω drivers.

PCB jumpers permit the selection of an ECL monostable prior to each ECL to TTL converter. These may be required if the pulse lengths would otherwise be too short for the TTL circuitry. The pulse length is set to about 90 ns.

6 Computer interface card

This card contains two 8-bit and one 4-bit bidirectional buffers relaying a front panel 25-pin Cannon D connector to the chassis backplane. The directions of the buffers are set by PCB jumpers.

Two computer interface cards are required for connecting the crate to the control system. Further details are given in Section 7.

7 Computer control

Computer control of the crate is via the two rear-mounted Cannon 25-pin D connectors. They are designed to be connected to two VMOD TTL modules within a DSC chassis. These VME modules are standard AB control system hardware for TTL I/O. Data are written to and read from the crate byte by byte.

The pin assignments for the two connectors are given in Tables 2 and 3. Connector 1 contains the eight address inputs, A7 to A0 and the input data byte DIN7 to DIN0. Connector 2 contains the following:

a) Output data byte DOUT7 to DOUT0.

b) WRITE. Data are written to the chassis when WRITE is low. The address and data inputs should be stable from 20 ns before the high-to-low transition to 20 ns after the low-to-high transition. WRITE should be low for at least 50 ns.

c) READ. Data are read from the chassis when READ is low. The address and data inputs should be stable from 20 ns before the high-to-low transition to 20 ns after the low-to-high transition. READ should be low for at least 50 ns.

d) LOCAL. HIGH = local control. LOW = computer control of chassis. However, computer data can be written to and read from the chassis irrespective of the state of this bit.

The format of the address byte is given in Table 4. The three most significant bits are used to address the counter drawer, of which there will be a maximum of four in the chassis. The five least significant bits address one of the 18 8-bit latches in each drawer.

The data format for the first byte is given in Table 5. It is used for selecting the trigger source and disabling the counters. Byte 2 (Table 6) contains the least significant bit of the fine delay (10 ps) steps for the four counters. The 8 most significant bits of fine delay for counters 1, 2, 3, and 4 are in bytes 3, 7, 11 and 15 respectively (Table 7). The remaining bytes (Tables 8 to 10) contain the 24-bit counter delays.

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	A0	10	GND	19	DIN3
2	A2	11	UNUSED	20	DIN1
3	A4	12	UNUSED	21	GND
4	A6	13	GND	22	A7
5	GND	14	UNUSED	23	A5
6	DIN0	15	UNUSED	24	A3
7	DIN2	16	GND	25	A1
8	DIN4	17	DIN7		
9	DIN6	18	DIN5		

Table 2: Pin assignment for connector 1.

PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL	PIN NUMBER	SIGNAL
1	DOUT0	10	GND	19	UNUSED
2	DOUT2	11	UNUSED	20	READ
3	DOUT4	12	UNUSED	21	GND
4	DOUT6	13	GND	22	DOUT7
5	GND	14	UNUSED	23	DOUT5
6	WRITE	15	UNUSED	24	DOUT3
7	LOCAL	16	GND	25	DOUT1
8	UNUSED	17	UNUSED		
9	UNUSED	18	UNUSED		

Table 3: Pin assignment for connector 2.

ADDRESS BITS								
A7	A6	A5	A4	A3	A2	A1	AO	
0	0	0	X	X	X	X	X	DRAWER 1
0	0	1	X	X	X	X	X	DRAWER 2
0	1	0	X	X	X	X	X	DRAWER 3
0	1	1	X	X	X	X	X	DRAWER 4
X	X	X	0	0	0	0	0	BYTE 1, TRIGGER SELECT AND DISABLE
X	X	X	0	0	0	0	1	BYTE 2, 10 ps STEPS, ALL FOUR COUNTERS
X	X	X	0	0	0	1	0	BYTE 3, COUNTER 1 FINE DELAY
X	X	X	0	0	0	1	1	BYTE 4, COUNTER 1 BITS 0 TO 7
X	X	X	0	0	1	0	0	BYTE 5, COUNTER 1 BITS 8 TO 15
X	X	X	0	0	1	0	1	BYTE 6, COUNTER 1 BITS 16 TO 23
X	X	X	0	0	1	1	0	BYTE 7, COUNTER 2 FINE DELAY
X	X	X	0	0	1	1	1	BYTE 8, COUNTER 2 BITS 0 TO 7
X	X	X	0	1	0	0	0	BYTE 9, COUNTER 2 BITS 8 TO 15
X	X	X	0	1	0	0	1	BYTE 10, COUNTER 2 BITS 16 TO 23
X	X	X	0	1	0	1	0	BYTE 11, COUNTER 3 FINE DELAY
X	X	X	0	1	0	1	1	BYTE 12, COUNTER 3 BITS 0 TO 7
X	X	X	0	1	1	0	0	BYTE 13, COUNTER 3 BITS 8 TO 15
X	X	X	0	1	1	0	1	BYTE 14, COUNTER 3 BITS 16 TO 23
X	X	X	0	1	1	1	0	BYTE 15, COUNTER 4 FINE DELAY
X	X	X	0	1	1	1	1	BYTE 16, COUNTER 4 BITS 0 TO 7
X	X	X	1	0	0	0	0	BYTE 17, COUNTER 4 BITS 8 TO 15
X	X	X	1	0	0	0	1	BYTE 18, COUNTER 4 BITS 16 TO 23

Table 4: Address format.

DATA BITS								
D7	D6	D5	D4	D3	D2	D1	DO	
X	X	X	X	X	1	1	1	TRIGGER 1 SELECTED
X	X	X	X	X	1	1	0	TRIGGER 2 SELECTED
X	X	X	X	X	1	0	1	TRIGGER 3 SELECTED
X	X	X	X	X	1	0	0	TRIGGER 4 SELECTED
X	X	X	X	X	0	0	0	FRONT PANEL TRIGGER SELECTED
X	X	X	X	0	X	X	X	COUNTER 1 DISABLED
X	X	X	X	1	X	X	X	COUNTER 1 ENABLED
X	X	X	0	X	X	X	X	COUNTER 2 DISABLED
X	X	X	1	X	X	X	X	COUNTER 2 ENABLED
X	X	0	X	X	X	X	X	COUNTER 3 DISABLED
X	X	1	X	X	X	X	X	COUNTER 3 ENABLED
X	0	X	X	X	X	X	X	COUNTER 4 DISABLED
X	1	X	X	X	X	X	X	COUNTER 4 ENABLED

Table 5: Data format for byte 1.

DATA BITS								
D7	D6	D5	D4	D3	D2	D1	DO	
X	X	X	X	X	X	X	1	COUNTER 1 10 ps INCREMENT OFF
X	X	X	X	X	X	X	0	COUNTER 1 10 ps INCREMENT ON
X	X	X	X	X	X	1	X	COUNTER 2 10 ps INCREMENT OFF
X	X	X	X	X	X	0	X	COUNTER 2 10 ps INCREMENT ON
X	X	X	X	X	1	X	X	COUNTER 3 10 ps INCREMENT OFF
X	X	X	X	X	0	X	X	COUNTER 3 10 ps INCREMENT ON
X	X	X	X	1	X	X	X	COUNTER 4 10 ps INCREMENT OFF
X	X	X	X	0	X	X	X	COUNTER 4 10 ps INCREMENT ON

Table 6: Data format for byte 2.

DATA BITS								DELAY, ps (approximate)
D7	D6	D5	D4	D3	D2	D1	DO	
1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	0	20
1	1	1	1	1	1	0	1	40
↓	↓	↓	↓	↓	↓	↓	↓	↓
0	0	0	0	0	0	1	0	5060
0	0	0	0	0	0	0	1	5080
0	0	0	0	0	0	0	0	5100

Table 7: Data format for bytes 3, 7, 11 and 15 (20 ps steps).

DATA BITS								DELAY, CLOCK PERIODS
D7	D6	D5	D4	D3	D2	D1	DO	
1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	0	1	2
↓	↓	↓	↓	↓	↓	↓	↓	↓
0	0	0	0	0	0	1	0	253
0	0	0	0	0	0	0	1	254
0	0	0	0	0	0	0	0	255

Table 8: Data format for bytes 4, 8, 12 and 16 (1 period steps).

DATA BITS								DELAY, CLOCK PERIODS
D7	D6	D5	D4	D3	D2	D1	DO	
1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	0	256
1	1	1	1	1	1	0	1	512
↓	↓	↓	↓	↓	↓	↓	↓	↓
0	0	0	0	0	0	1	0	64768
0	0	0	0	0	0	0	1	65024
0	0	0	0	0	0	0	0	65280

Table 9: Data format for bytes 5, 9, 13 and 17 (256 period steps).

DATA BITS								DELAY, CLOCK PERIODS
D7	D6	D5	D4	D3	D2	D1	DO	
1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	0	65536
1	1	1	1	1	1	0	1	131072
↓	↓	↓	↓	↓	↓	↓	↓	↓
0	0	0	0	0	0	1	0	16580608
0	0	0	0	0	0	0	1	16646144
0	0	0	0	0	0	0	0	16711680

Table 10: Data format for bytes 6, 10, 14 and 18 (65536 period steps).

8 Documentation

Circuit diagrams, PCB layout, front panel drawings and other documentation on this crate can be found in the EDMS database under the following item names:

- 24-bit counter main PCB CERN-0000008594
- 24-bit counter front panel CERN-0000010236
- Computer interface EDA-00672
- Fan-out and combiner CERN-0000010377
- Converter CERN-0000010375
- Backplane A (front) EDA-00285
- Backplane B (rear) EDA-00286

9 References

[1] G. Geschonke and A. Ghigo (editors), “CTF3 design report”, CERN/PS 2002-008 (RF).

[2] P. Fernier, J. Serrano, “The CTF3 Delay Card, An 8-channel VME module to delay TTL pulses in 200 ps steps”, PS/CO/Note 2001-014 (Tech.).